

1 151. (Twice Amended) A method of operation of a synchronous memory
2 device, wherein the memory device includes an array of memory cells,
3 the method of operation comprises:

4 receiving an external clock signal;

5 receiving block size information, wherein the block size
6 information defines an amount of data to be output by the memory device
7 in response to a first operation code;

8 sampling the first operation code synchronously with respect to
9 the external clock signal wherein the first operation code instructs
10 the memory device to perform a read operation; and

11 outputting the amount of data in response to the first operation
12 code.

1 2 1 152. (Twice Amended) The method of claim 151 wherein the block
2 size information also defines an amount of data to be input by the
3 memory device, wherein the amount of data is input in response to a
4 second operation code, and wherein the second operation code instructs
5 the memory device to perform a write operation, the method further
6 including:

7 sampling the second operation code synchronously with respect to
8 a transition of the external clock signal; and

9 inputting the amount of data in response to the second operation
10 code.

1 6 1 153. (Twice Amended) The method of claim 151 wherein the memory
2 device samples the block size information synchronously with respect to
3 the external clock signal.

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1 161. (Twice Amended) The method of claim 151 wherein the block
2 size information is an encoded value and wherein the block size
3 information is sampled synchronously with respect to a rising or
4 falling edge of the external clock signal.

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1 165. (Twice Amended) A method of controlling a synchronous memory
2 device by a controller, wherein the memory device includes an array of
3 memory cells, the method of controlling the memory device comprises:
4 issuing block size information to the memory device synchronously
5 with respect to an external clock signal, wherein the block size
6 information defines an amount of data to be output by the memory
7 device; and
8 issuing a first operation code to the memory device synchronously
9 with respect to the external clock signal, wherein the first operation
10 code instructs the memory device to perform a read operation.

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1 176. (Twice Amended) A synchronous dynamic random access memory
2 device having at least one memory section including a plurality of
3 memory cells, the memory device comprising:
4 clock receiver circuitry to receive an external clock signal;
5 input receiver circuitry, including a first plurality of input
6 receivers to sample block size information synchronously with respect
7 to the external clock signal, wherein the block size information
8 defines an amount of data to be output by the memory device in response
9 to a first operation code; and

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a plurality of output drivers to output the amount of data in response to the first operation code.

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- 1 *29* 179. (Twice Amended) The memory device of claim *176* wherein the
2 input receiver circuitry samples the first operation code synchronously
3 with respect to the external clock signal.
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